AMENDMENTS TO THE SPECIFICATION AND ABSTRACT

Please amend the paragraph [0006] beginning on page 3, line 2 as follows:

[0006] However, it is inconvenient for users that connectable electric apparatuses are limited according to their available supply current, and there has been a call for an applicable memory card drive independent of the amount of current able to be supplied by an electric apparatus to which the memory card drive is connected.

———The present invention has been made in view of the problem above, and aims at offering a recording device and a memory card drive device capable of changing their operating conditions according to the amount of current that can be supplied by an electric apparatus to which the recording device or the memory card drive device is connected, and controlling their consumption current to be at or below the available supply current of the electric apparatus.

Please amend the paragraph [0007] beginning on page 3, line 17 as follows:

[0007] In order to achieve the above stated objective, the present invention is a recording device comprising: one or more semiconductor memories; an obtaining unit operable to obtain an upper limit of current to be supplied from an accessing apparatus to the recording device; a command obtaining unit operable to obtain from the accessing apparatus at least one command, a type of which is one of a write command instructing data writing to the semiconductor memories and a read command instructing data reading from the semiconductor memories~~a command instructing access to the semiconductor memories~~; an access unit operable to receive current supply from the accessing apparatus and access the semiconductor memories according to a ~~one or more~~ control ~~signals~~ signal; and a control unit operable to calculate an access upper limit by subtracting the amount of current consumed by individual units other than the semiconductor memories and the access unit from the upper limit, set operating conditions of the access unit and the semiconductor memories according to the type of the obtained command, using the access upper limit, generate the control signal ~~signals~~ based on the obtained command and the operating conditions, and output the control ~~signals~~ signal.

Please amend the paragraph [0009] beginning on page 4, line 12 as follows:

[0009] According to the structure above, the recording device of the present invention sets the

operating conditions based on the access upper limit which is calculated from the upper limit obtained from the accessing apparatus. Accordingly, by setting appropriate operating conditions, the present invention enables access to the semiconductor memories, requiring electric current no more than the amount supplied by the accessing device.

The recording device above is characterized by: the control unit prestoring therein a current consumption value representing the amount of current consumed by the access unit and the semiconductor memories, with respect to each type of the write and the read commands ~~in association with the command~~, and setting the operating conditions corresponding to the type of the obtained command using the access upper limit and the current consumption value.

Please amend the paragraph [0011] beginning on page 5, line 8 as follows:

[0011] The recording device above is characterized by: the control unit setting the operating conditions so that cause a parallel-operation count of memories out of the semiconductor memories to operate in parallel, and outputting to the access unit the control signal ~~signals~~ generated based on the obtained command and the operating conditions, and instructing access to the parallel-operation count of memories; and the access unit accesses ~~accessing~~ the parallel-operation count of memories. Here, the parallel-operation count is smaller than or equal to number of pieces of all the semiconductor memories.

Please amend the paragraph [0012] beginning on page 5, line 8 as follows:

[0012] According to the structure above, the control unit sets the operating conditions so that the parallel-operation ~~count of~~ memories, which are selected from among the semiconductor memories of the recording device, ~~out of the semiconductor memories~~ operate in parallel. Here, the number of the parallel-operation memories matches the number of all or some of the semiconductor memories. That is, the number of semiconductor memories for parallel operations is ~~limitd~~ limited. The amount of current consumed by the recording device corresponds to the number of semiconductor memories in the parallel operations. Therefore, limiting the number of semiconductor memories for the parallel operations guarantees reliable restriction of the amount of current consumed by the recording device.

Please amend the paragraph [0014] beginning on page 6, line 11 as follows:

[0014] The recording device above is characterized by: the access unit ~~control signals each~~ including as many access subunits as the semiconductor memories, and each of the access subunits corresponding to a different one of the semiconductor memories; the control unit generating the control signal that includes as many access signals as the parallel-operation count of memories; each of the access signals being for instructing a different one of the access subunits to access a corresponding semiconductor memory thereof; the control unit outputting each of the access signals to a corresponding one of the access subunits; and access subunits that received the access signals accessing corresponding semiconductor memories according to the received access signals. ~~a memory information piece specifying one of the semiconductor memories; the control unit sequentially outputting the control signals; and the access unit receiving each of the control signals and accessing a semiconductor memory specified by the memory information piece.~~

Please amend the paragraph [0015] beginning on page 6, line 17 as follows:

[0015] According to the structure above, the control unit ~~sequentially~~ outputs each access signal to a different one of the access subunits, and the access subunits that received the access signals have access to the corresponding semiconductor memories. Therefore, sequentially outputting access instructions to the respective access units enables data to be written to the semiconductor memories of the recording device in rotation, which allows the respective semiconductor memories to store therein a more or less even amount of data. This ~~the control signals, each of which includes a memory information piece specifying one of the semiconductor memories, and the access unit receives each of the control signals and has access to a semiconductor memory specified by the memory information piece included in the received control signal. Thus, sequentially writing data to the semiconductor memories of the recording device~~ avoids a reduction in the number of semiconductor memories operable in parallel. Accordingly~~Herewith~~, a decrease in access speed of the recording device can be prevented.

Please amend the paragraph [0016] beginning on page 6, line 28 as follows:

[0016] The recording device of the present invention ~~above~~ is characterized by: the control unit setting the operating conditions ~~so~~ that cause the semiconductor memories to operate at a memory frequency which is no more than a maximum operating frequency of the semiconductor

memories, generating a clock signal having the ~~a~~ same frequency as the memory frequency based on the command and the operating conditions, and outputting to the access unit the control signal ~~signals each~~ including the generated clock signal; and the access unit outputting the clock signals received from the control unit to the semiconductor memories and has access to ~~accesses~~ the semiconductor memories.

Please amend the paragraph [0018] beginning on page 7, line 26 as follows:

[0018] The recording device of the present invention ~~above~~ is characterized by: the control unit prestoring therein, as the current consumption value, a maximum current value which represents the amount of current consumed by the access unit and the semiconductor memories when each of the semiconductor memories operates at the maximum operating frequency, and calculating the memory frequency using the access upper limit and the ratio of the maximum operating frequency to the maximum current value.

According to the structure above, the control unit can readily calculate the operating frequency using the access upper limit and the ratio of the maximum operating frequency to the maximum current value.

Please amend the paragraph [0019] beginning on page 8, line 10 as follows:

[0019] The recording device of the present invention ~~above~~ is characterized by: the control unit prestoring therein the maximum operating frequency together with the maximum current value.

According to the structure above, the control unit prestores the maximum operating frequency together with the maximum current value, and is therefore able to calculate the operating frequency promptly.

In addition, the control unit prestores therein the current consumption value associated with the read command, ~~that instructs data reading,~~ and sets the operating conditions that causes ~~so that~~ the semiconductor memories to operate at the memory frequency in response to the read command ~~instructing the data reading~~.

Please amend the paragraph [0021] beginning on page 9, line 8 as follows:

[0021] The recording device of the present invention ~~above~~ is characterized by: the control unit including a frequency divider, generating the clock signal having the same frequency as the

memory ~~maximum operating~~ frequency using the frequency divider, and outputting the control signal ~~signals each~~ including the generated clock signal.

According to the structure above, the control unit is capable of readily changing the frequency of the clock signal using the frequency divider.

Please amend the paragraph [0022] beginning on page 9, line 16 as follows:

[0022] In addition, the control unit may include a PLL (Phase Lock Loop), generate the clock signal having the same frequency as the memory ~~maximum operating~~ frequency using the PLL, and output the control signal ~~signals each~~ including the generated clock signal.

According to the structure above, the control unit can continuously change the frequency of the clock signal using the PLL. As a result, the control unit is capable of generating and outputting the clock signal having the best suited frequency for the access upper limit and the command obtained by the command obtaining unit.

Please amend the paragraph [0023] beginning on page 9, line 27 as follows:

[0023] The recording device of the present invention is characterized by: the control unit setting, as the operating conditions, a 1st operating condition that causes ~~in which~~ a parallel-operation count of memories out of the semiconductor memories to operate in parallel and a 2nd operating condition that causes ~~in which~~ the semiconductor memories to operate at an operating frequency no more than a maximum operating frequency of the semiconductor memories, adopting at least one of the 1st and 2nd operating conditions based on the type of the obtained command, and generating the control signal ~~signals~~ based on the adopted operating condition.

Please amend the paragraph [0025] beginning on page 10, line 20 as follows:

[0025] The semiconductor memories of the recording device of the present invention may be ~~is characterized by: the semiconductor memories being~~ flash memories.

———Flash memories are today widely in use and a lot of practical achievements in producing flash memories have already been made. Therefore, the recording device having the above-mentioned structure can easily be produced.

———The semiconductor memories of the recording device of the present invention may be nonvolatile magnetic memories.

Please amend the paragraph [0028] beginning on page 11, line 20 as follows:

[0028] According to the structure above, the recording device comprises portable semiconductor memories and a memory card drive device. Thus, the memory card drive device allows for high-speed data input and output, using existing, commercially available memory cards as the portable semiconductor memories.

The recording device of the present invention is characterized by: the control unit outputting the control signal ~~signals each~~ including a clock signal; and the access unit supplying the clock signal only to one or more of the semiconductor memories being accessed, and stopping supply of the clock signal to remaining one or more of the semiconductor memories being not accessed.